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EXAMINER	
BRADLEY, MATTHEW A	
ART UNIT	**PAPER NUMBER**
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/798,641	EILERT, SEAN S.	
	Examiner	Art Unit	
	Matthew Bradley	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,11-14 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,11-14 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's election of 1-7 and 11-14 in the reply filed on 7 November 2007 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Applicant's arguments have been carefully and fully considered but they are not persuasive. Accordingly, this action has been made FINAL.

Claim Status

Claims 1-7, 11-14, and 32 remain pending and are ready for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims **1-6**, **11**, and **14** are rejected under 35 U.S.C. 102(b) as being anticipated by Wang (U.S. 6,449,625) hereinafter referred to as Wang.

As per independent claim **1**, Wang teaches,

- A stack having a stack depth configured in a nonvolatile memory to store parameter values, where each memory write invalidates previous data (Column 1 lines 48-51; Column 4 lines 46-47).

As per dependent claim **2**, Wang teaches,

- The stack of claim 1 wherein the nonvolatile memory includes a pair of blocks that are erased independently (Column 2 lines 30-34). *The Examiner notes that the inherent characteristic of a stack is that the blocks are able to be erased – independently. Accordingly, Wang teaches the instant limitation with the recitation of stack and its characteristics.*

As per dependent claim **3**, Wang teaches,

- The stack of claim 2 wherein valid parameter values are stored in a first block of the pair of blocks and a second block is erased (Column 2 lines 33-46). *The Examiner notes that the process of garbage collection on the stack provides for the erasure of blocks as instantly claimed.*

As per dependent claim **4**, Wang teaches,

- The stack of claim 3 wherein valid parameter values are stored in the second block of the pair of blocks and the first block is erased (Column 2 lines 33-46). *The Examiner notes that with respect to the comments made supra in claim 3, the garbage collection process is able to identify blocks that are 'stale.' As such, the first block of the non-volatile memory can contain blocks that will be erased as shown in Figures 5A-5F.*

As per dependent claim **5**, Wang teaches,

- The stack of claim 1 further including a register to store an offset value used to generate an address for words in the nonvolatile memory (Column 4 lines 39-41). *The Examiner notes that use of numerically addressable blocks within the nonvolatile memory allows for the operation of a stack to be realized. As taught in Column 4 lines 15-26, the flash memory logs all transactions. Accordingly, the use of addressable blocks and the act of keeping a log of all transactions, teaches the instant limitation of a register used to store values.*

As per dependent claim **6**, Wang teaches,

- The stack of claim 1 further including a smart stack controller to dynamically determine a number of blocks used in the stack (Column 3 lines 25-39).

As per independent claim **11**, Wang teaches,

- A nonvolatile stack to store parameter values in words of a nonvolatile memory where a write of the nonvolatile stack invalidates previous instructions or data stored in the nonvolatile stack (Column 1 lines 48-51; Column 4 lines 46-47).

As per dependent claim **14**, Wang teaches,

- The nonvolatile stack of claim 11 wherein the nonvolatile memory maps a received address to determine memory blocks to be written (Column 4 lines 26-47).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **7** and **12-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Jou et al (U.S. 5,568,423) hereinafter referred to as Jou.

As per dependent claim **7**, Wang teaches the limitations of independent claim 1 from which dependent claim 7 depends upon as noted supra.

Wang fails to explicitly teach the use of a smart stack controller for the purpose of distributing write cycles.

Jou teach, further including a smart stack controller to distribute write cycles across multiple blocks of the nonvolatile memory (Column 2 lines 20-48 of Jou). *The Examiner notes herein that the algorithm used in Jou to evenly distribute the write cycles anticipates the instant limitation of a smart stack controller.*

Wang and Jou are analogous art because they are from the same field of endeavor, namely FLASH memory devices.

At the time of invention it would have been obvious to one of even rudimentary skill in the art, having both the teachings of Wang and Jou before him/her, to combine the algorithm of Jou into Wang for the benefit of

guaranteeing that each and every block is used thus lessening the chance of premature failure of the blocks.

The suggestion for doing so would have been that, "the wear leveling system of the present disclosure, will operate to guarantee that the usage of each and ever block within the flash memory address space will be equally utilized or fairly distributed (Column 2 lines 27-31 of Jou).

Therefore, it would have been obvious to combine Wang with Jou for the benefit of guaranteeing that each and every block is used thus lessening the chance of premature failure of the blocks to obtain the invention as specified in claims 7 and 12-13.

As per dependent claim **12**, the combination of Wang and Jou teach,

- The nonvolatile stack of claim 11 wherein a memory pool in at least first and second blocks of the nonvolatile memory are sized to balance cycling and data retention capabilities with a write specification (Column 2 lines 20-48 of Jou).

As per dependent claim **13**, the combination of Wang and Jou teach,

- The nonvolatile stack of claim 11 further including a stack controller to distribute write cycles across multiple blocks of the nonvolatile memory (Column 2 lines 20-48 of Jou).

Claim **32** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view Royer JR et al (U.S. 2003/0061436), hereinafter referred to as Royer.

As per dependent claim **32**, Wang teaches the limitations of independent claim 1 from which dependent claim 8 depends upon as noted supra.

Wang fails to teach, wherein the nonvolatile memory is a polymer memory that includes ferroelectric memory cells.

Royer teach, wherein the nonvolatile memory is a polymer memory that includes ferroelectric memory cells (Paragraph 0015).

Wang and Royer are analogous art because they are from the same field of endeavor, namely non-volatile memory.

At the time of invention it would have been obvious to one of ordinary skill in the art, having both the teachings of Wang and Royer before him/her, to implement the non-volatile memory of Wang in polymer memory devices because polymer memory devices are easy to manufacture, provide a large capacity non-volatile memory array, and are also inexpensive.

The motivation for doing so would have been that, "they are simpler to manufacture, as well as denser in populations. This provides a large capacity, nonvolatile memory array that is not very expensive (Paragraph 0016 of Royer)."

Therefore it would have been obvious to combine Wang with Royer for the benefit of a easy to manufacture, large capacity non-volatile memory array that is inexpensive, to obtain the invention as specified in claim 32.

Response to Arguments

Applicant's arguments filed as part of the response on 17 November 2006 have been carefully and fully considered but they are not persuasive.

With respect to Applicant's argument located within the third full paragraph of the third page of the remarks (numbered as page 10) which recites:

> *"A first feature not taught by Wang that is included in Applicant's claim 1 is the feature that the stack stores parameter values."*

The Examiner respectfully disagrees. First, the Examiner wishes to draw attention to the language, "configured ... to store" as presently found in the claims. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

As shown in the MPEP, 2106,

> *"Language that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation. The following are examples of language that may raise a question as to the limiting effect of the language in a claim:*
> *(A) statements of intended use or field of use,*
> *(B) "adapted to" or "adapted for" clauses,*
> *(C) "wherein" clauses, or*
> *(D) "whereby" clauses."*

Thus, the language 'configured to' does not further limit the claim in that such language represents intended use.

With respect to Applicant's argument located within the fourth full paragraph of the third page of the remarks (numbered as page 10) which recites:

> *"A second feature not taught by Wang that is included in Applicant's claim 1 is the feature that each memory write invalidates previous data."*

The Examiner respectfully disagrees. Applicant's argue that, "Wang teaches a write cycle to perform numerous data transfers of Ram data to the FLASH

memory, followed by a garbage collection cycle to clean up the FLASH. Wang's two staged algorithm of a write cycle and a garbage collection cycle does not teach Applicant's claimed limitation that each memory write invalidates previous data." The Examiner wishes to draw attention to Column 4 line 46 to at least Column 5 line 16. The Examiner notes that Wang teaches that the 'purpose of the garbage collection cycle ... is to only maintain or preserve records of those transactions that represent the most recent action preformed on any particular record.' Further Wang teaches in Column 8 lines 55-65 with respect to figure 4(d) that, 'At the conclusion of the garbage collection cycle represented by FIG. 4(d), preserved data will have been pushed to the bottom of the downward facing stack.' Thus, when new data is written to the stack, the garbage collection cycle is immediately preformed and the preserved data is pushed to the bottom of the stack as well as the system of Wang no longer retaining the older data corresponding to the newer data. In the act of pushing the preserved data to the bottom of the stack, the data that is being overwritten, previous data, is being invalidated as instantly claimed.

Applicant's appear to be arguing that since Wang teaches a write cycle and then a garbage collection cycle, that this two staged algorithm does not teach Applicant's claimed invention. The Examiner wishes to further note that at least insofar as it appears to be clear that there is no claim language that prevents such two staged algorithm from occurring. Thus, as is shown in the rejection and comments made *supra* Wang teaches that which is instantly claimed.

NOTE: In the 'Notice to the Applicant regarding a Non-Complaint Amendment' mailed 19 September 2006, the Examiner noted that the replacement Abstract must be presented on a separate sheet. In the response to the Notice filed 17 November 2006, Applicant's state that the Abstract of the disclosure has been modified to overcome the Examiner's objection. The Examiner has been unable to locate the modified Abstract and requests that it be filed so that it may be placed of record in the file.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Bradley whose telephone number is (571) 272-8575. The examiner can normally be reached on 6:30-3:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DAS/mb MB

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SUPERVISORY PATENT EXAMINER